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13. ABSTRACT *(Maximum 200 words)*

The aim of this programme is to prepare, evaluate and optimise Total Dielectric Isolated (TDI) structures in order to develop the technology for the preparation of substrates for circuits which exhibit improved radiation tolerance.

The work carried out during this reporting period has provided a sound base for this project. Successful experiments include the preparation of device worthy substrates in variously patterned wafers, identification of the microstructure of TDI wafers by cross-sectional transmission electron microscopy (XTEM) and the successful implementation of a new predictive software package (IRIS). In addition a new halogen lamp heated wafer holder (funded under another contract) has been commissioned and used to prepare substrates with pre-heating and background heating up to 680°C. Keywords: Silicon (KW)

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UNIVERSITY OF SURREY

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

TOTAL DIELECTRIC ISOLATION (TDI) OF FULLY DEPLETED DEVICE STRUCTURES

AFOSR-88-0356
P L F Hemment
July 1990

Programme Manager:
Dr D Eirug Davies

INTERIM SCIENTIFIC REPORT

SUMMARY

SIMOX is the most mature SOI technology and many laboratories in the USA, Japan and Europe are developing radiation hard and nigh speed CMOS/SIMOX circuits. However, circuits fabricated on conventional SIMOX substrates still require additional processing (eg MESA etching or LOCOS) to achieve lateral device isolation.

The innovative programme of work undertaken at the University of Surrey is designed to take SIMOX technology a stage further by achieving both vertical and lateral isolation during a single O^+ ion implantation stage. The process being developed, known as Total Dielectric Isolation (TDI), achieves this goal by implanting into a patterned wafer and thereby synthesising a non-planar buried layer of SiO_2, which completely isolates the silicon island from the underlying substrate. The technique has already been demonstrated and dielectrically isolated islands have been formed.

The principal achievements during the current period are (i) results of microstructural analysis of TDI structures by ross-section transmission electron microscopy (XTEM), (ii) completion of a computer model which permits the dimensions (t_{Si}, T_{SiO_2}) to be predicted in both "as implanted" and annealed substrates, and (iii) first results of experiments to planarise the top (free) silicon surface).

The project has benefitted from close collaborative links with staff at NRL, Washington DC, and IBIS Technology Corp, Danvers, MA.

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1. REPORT OF WORK COMPLETED

A novel isolation technique (total dielectric isolation - TDI) to replace MESA etching and LOCOS isolation has been developed at the University of Surrey, which has twelve years experience in SIMOX technology. The TDI process is an extension of SIMOX technology and entails O^+ implantation through a patterned masking layer (SiO_2). As the ions lose energy within the mask a non-planar layer of SiO_2 may be synthesised which, by careful optimisation of the processing parameters, provides lateral and vertical isolation of the silicon device islands. The dimensions of the silicon islands are freely defined across the wafer by lithography from μm to mm. The islands are delineated by Si/SiO_2 interfaces which are formed by internal oxidation and have a topography quite different from previous structures and, thus, offer the prospect of forming novel structures and achieving improved radiation tolerance, which currently is necessary to meet system requirements. The dielectric isolation will also ensure circuit operation in high temperature environments, as reported for conventional SOI/CMOS.

The aim of the DOD programme is to prepare, evaluate and optimise TDI substrates for circuits with improved radiation hardness and substrates have been prepared and sent to NRL, Washington DC. The grant supports an experienced research fellow (Dr U Bussmann) and at the start of the project he was able to quickly define structures for the first round of experiments. Masked wafers were prepared by NRL, implanted at Surrey and returned to Washington for processing. In parallel the research fellow has developed techniques and expertise to enable him to optimise the TDI structures. This work has entailed the use of cross-sectional TEM to determine the lateral dimensions and microstructure of the silicon islands and interfaces, surface analysis techniques for composition and thickness determinations and development of a computer model (IRIS) to simulate the evolution of the oxide layer. The ideal TDI wafer will have a planar surface and this model, which incorporates r swelling, sputtering and diffusion, has been used to determine the optimum values of the processing parameters (energy, dose, mask thickness and etch back) to achieve this end.

The accomplishments and research progress during this period fall under

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the following headings.

1.1 Preparation of Substrates

Wafers were received from NRL with patterned masking layers and were implanted over a range of O^+ doses at 200 keV and substrate temperature of 550°C. These were used for materials science experiments. Further substrates with FET test patterns etched in the poly-silicon masking layer have been prepared and returned to NRL for annealing and fabrication of test devices.

Additional wafers with a LOCOS patterned masking layer have been implanted and studied in order to optimise the processing to achieve a planar surface after O^+ implantation.

1.2 Heated Sample Holder

Extensive testing of a new heated sample holder (funded under a separate contract) have been successfully completed and the facility is now available for implants in the temperature range 300°C to 700°C into 3" and 6" wafers.

The temperature has been calibrated and the facility is now used routinely to prepare substrates.

1.3 Materials Science Experiments

The microstructure of both "as implanted" and high temperature annealed samples have been studied by cross-sectional transmission electron microscopy (XTEM). A wide range of experimental conditions have been explored including implantations into thick and thin masking layers and the use of poly-silicon and oxide masks. The output from this work has been used to optimise the processing of wafers for test devices and as input to the computer simulation software.

1.4 Computer Simulations

The computer programme, IRIS, developed as part of this project, has been further extended to model the effect of high temperature annealing when the evolved oxygen depth profile is transformed into a rectangular distribution. This software is now running and has been used extensively to accurately predict the structure of device grade substrates.

2. FUTURE WORK

Priorities during the next period will be;

(i) description of the microstructure of TDI structures formed on LOCOS masked wafers,

(ii) optimisation of the processing conditions,

(iii) direct formation of thin film SIMOX/TDI substrates using lower energy O^+ ions and the heated sample holder, and

(iv) refinement of the computer model (IRIS) to extend the working range.

PUBLICATIONS

1. U Bussmann and P L F Hemment, "Computer Simulation of High Fluence Oxygen Profiles in Silicon", Nucl Inst & Meths B47, (1990), 22-28.

2. U Bussmann and P L F Hemment, "Layer Thickness Calculations for SOI Structures Formed by Oxygen Implantation", Accepted for publication in Appl Phys Letts.

3 U Bussmann, "Computer Modelling of Oxygen Distributions in SIMOX Substrates", Proc IV Inter Symp on SOI Technology and Devices, Ed: Dennis N Schmidt, Electrochem Soc Proc, Vol 90-6, 85, 1990.

4. U Bussmann, A K Robinson and P L F Hemment, "Energy and Dose Dependence of Si Top Layer and Buried Oxide Layer Thicknesses in SIMOX Substrates". Accepted by IIT'90, University of Surrey, July 1990.

5. U Bussmann, P L F Hemment, A K Robinson and V Starkov, "Oxygen Implantation Through Patterned Masks: A Method for Forming Insulating Silicon Device Islands Maintaining a Planar Surface", Accepted by IIT'90, University of Surrey, July 1990.

APPENDIX

- Reference 1 (above).
- Progress Reports 1, 2 and 3.

REPORT 1

AFOSR-88-0356

UNIVERSITY OF SURREY

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Total Dielectric Isolation (TDI) of Fully Depleted Device Structures

P L F Hemment
24th April 1989

PROGRESS REPORT

1. OBJECTIVE

The aim of this programme is to prepare, evaluate and optimise TDI structures as quickly as possible in order to develop the technology for the preparation of substrates which exhibit improved radiation tolerance.

2. TECHNICAL PROGRESS

The Research Fellow (Dr U Bussmann), supported by this contract, was appointed on time and rapid progress has been made in developing expertise and carrying out initial experiments. Technical progress will be reported under separate headings.

2.1 Computer Modelling

It is important to have predictive models to describe the movement of the free surface and buried interfaces during O^+ ion implantation. Software has been written which enables these movements to be followed in both the "window" and "field" regions of the structures, which are characterised by different sputtering rates.

The model uses an iterative procedure to simulate the evolution of the implanted oxygen depth profile. Input data is in the form of the concentration depth profile, either experimental or calculated using TRIM, of incremental doses of O^+ ions and the redistribution due to diffusion (if $x > 2$), swelling and sputtering is calculated after the addition of each increment of value, typically, 1×10^{15} O^+ cm^{-2}. The iterations are continued until the required dose has accumulated. Figures 1(b), (c) and (d) are calculated depth profiles of 1×10^{18} O^+ cm^{-2}, 1.4×10^{18} O^+ cm^{-2} and 1.8×10^{18} O^+ cm^{-2} implanted into silicon at an energy of 200 keV. Figures 1(f), (g) and (h) are the analogous profiles when the O^+ ions are implanted through a masking oxide of thickness 3200 Å. The rapid sputter erosion of the mask modifies the shape of the final distribution and increases the value of the critical dose required to achieve a stoichiometric oxide. These profiles, which have been calculated using values of the system variables derived from experiment, show good agreement with experimental profiles reported in the literature. Figures 1(a) and 1(e) show the oxygen distributions for a low dose of 1×10^{16} O^+ cm^{-2}.

2.2 Determination of Microstructure

The Research Fellow has access to a JEOL 200CX transmission electron microscope and an Ion Tech Fast Atom Beam Miller for detailed cross-sectional TEM (XTEM) studies of the TDI structures. A procedure for sample preparation has been developed and proven using TDI samples used in earlier experiments. The preparation of XTEM samples from the first batch of wafers will commence immediately after their return to Surrey after high temperature (1300°C, five hours) annealing at NRL.

The seventeen stage preparation procedure, resulting in samples of two different materials, is as follows:

Period	Action	Working Time (hours)
Day 1	1 Cleaving (15 - 20 pieces, 3 mm)	1.5
	2 Cleaning - Acetone → Methanol → Toluene	1
	3 Gluing - epoxy resin	1.5
Day 2	4 Mount between glass on stubs	1.5
	5 Coarse Polishing	2
	6 Fine Polish (SiC)	1
	7 First Diamond Polish (1 μm)	1
	8 Optical Check	0.5
	9 Reverse Sample Mount, Between Cover Slips	1.5
Day 3	10 Coarse Polishing	0.5
	11 Fine Polish (SiC)	1
	12 Fine Polish (1 μm)	1
	13 Optical Check	0.5
	14 Mount First Copper Grid	1
Day 4	15 Remove from Stub	1.5
	16 Mount Second Copper Grid	1.5
	TOTAL	18.5
Day 5	17 Commence Ion Milling (10 - 20 hours for each sample)	

--x--

Select sample for analysis

--x--

2.3 Implantation of Masked Wafers

A set of twelve 3" wafers has been received from the Naval Research Laboratory (NRL) which have patterned polysilicon masking layers of thickness 0.25 μm and 1.5 μm. Areas are defined which are suitable for analysis by Rutherford backscattering, SEM and TEM. The first batch of four wafers have been implanted at ≈550°C with 200 keV O^+ ions over the dose range 0.3×10^{18} O^+ cm^{-2} to 2.4×10^{18} O^+ cm^{-2}. Two of these implanted wafers have been sent to the NRL for capping and high temperature annealing and will be returned to Surrey for analysis.

2.4 Materials Science

A novel feature of the patterned TDI structures is that the formation of the synthesised dielectric layer can be dominated by different mechanisms in the window and field regions. If the sputter rate is high (eg SiO_2 masking layer) then the final oxygen depth distribution will be a "sputter limited profile" which may not achieve an adequately high volume concentration to directly form the stoichiometric silicon dioxide. It is important, therefore, to determine the dependence of the volume concentration upon sputter rate as this information is input data for the computer model (Section 2.1).

Figures 3(a) and (b) are the backscatter energy spectra of 1.5 MeV He^+ from a SIMOX sample (1.8×10^{18} O^+ cm^{-2}) and a masked sample (3200 Å of SiO_2) implanted with a dose of 1.7×10^{18} O^+ cm^2, respectively. The oxygen depth distributions and the composition of the buried oxide (SiO_x) can be inferred from the yield deficiency between channels 150 and 250, which is due to the included oxygen. These preliminary results suggest that the oxide formed beneath the mask (Figure 3(b)) is sub-stoichiometric, which is consistent with previous SIMS analyses. Further analyses will be carried out to improve the statistical significance of the results.

2.5 Heated Sample Holder

This TDI project draws upon the expertise of staff at Surrey and requires access to the ion implantation facilities. New equipment, which has recently been ordered and will be used by Dr Bussmann, includes a lamp heated sample holder. This unit will enable the wafer to be pre-heated to 500°C - 600°C and will provide background heating to maintain the wafer at a constant temperature during the three hours to five hours of implantation time. Dr Bussmann has participated in design and technical discussions with the manufacturer.

3. FUTURE WORKPLAN (APRIL - JUNE 1989)

The initial implantations have been carried out on time and during the next reporting period (April 1989 - June 1989) it will be possible to evaluate the TDI structures. This will entail the following activities.

FIGURE CAPTIONS

Figure 1: Calculated depth profiles of 1×10^{18} O^+ cm^{-2}, 1.4×10^{18} O^+ cm^{-2} and 1.8×10^{18} O^+ implanted at 200 keV into bulk silicon [(b), (c) and (d)] and into silicon through an SiO_2 mask of thickness 3200 Å [(f), (g) and (h)], respectively. Figures 1(a) and 1(e) show the low dose depth profiles.

Figure 2: Backscatter energy spectra of 1.5 MeV He^+ ions from (a) a SIMOX sample (1.8×10^{18} O^+ cm^{-2}, 200 keV) and (b) a masked sample (3200 Å, SiO_2) implanted with a dose of 1.7×10^{18} O^+ cm^{-2}, respectively. The residual oxide (≈500 Å) on the surface of the masked sample was removed before carrying out the analysis.

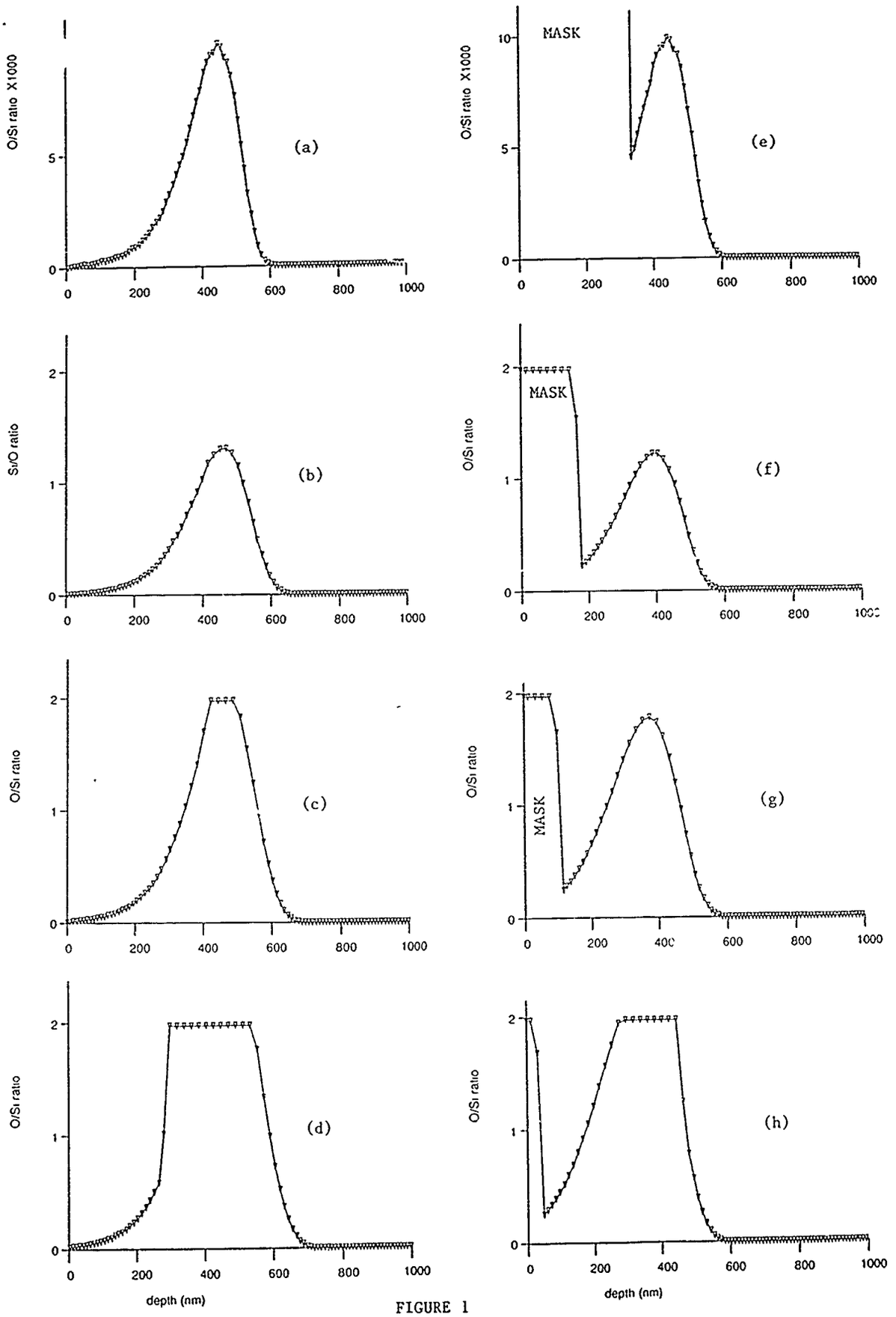
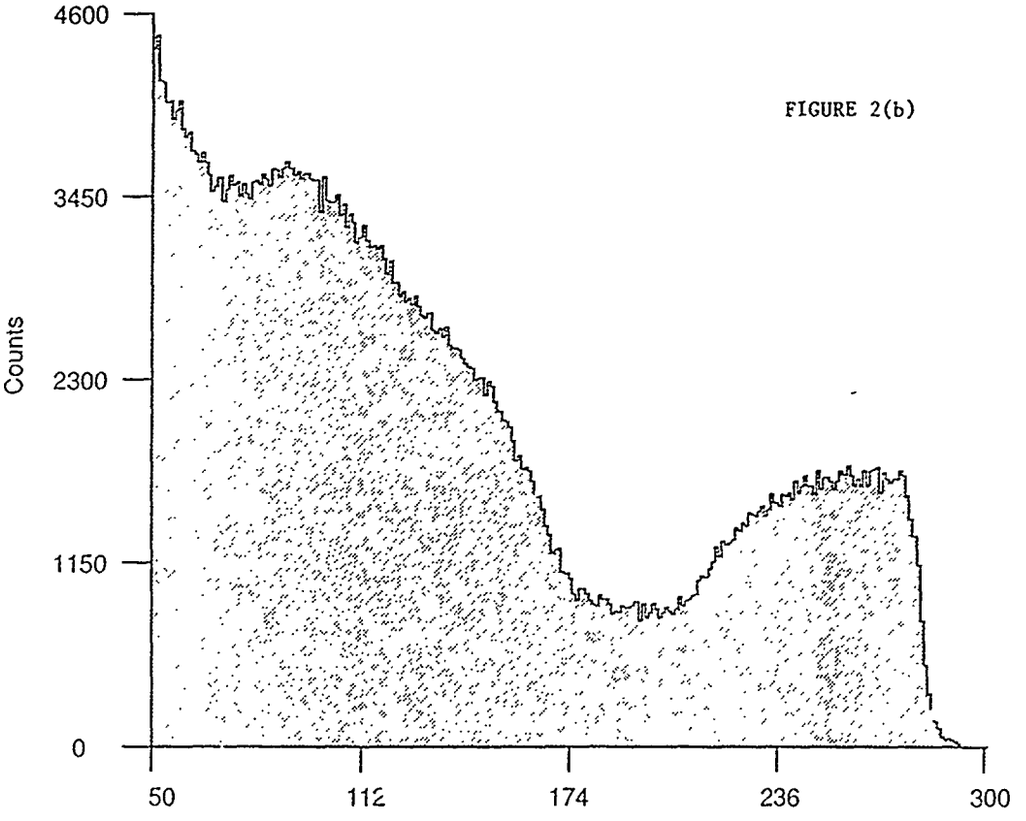

O/Si ratio X1000
(a)
MASK
(e)
Si/O ratio
(b)
O/Si ratio
MASK
(f)
O/Si ratio
(c)
MASK
(g)
O/Si ratio
(d)
(h)
depth (nm)
depth (nm)

FIGURE 1

FIGURE 2(b)



Channel Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	0	0	0	1	2452	4571	4447	4458	4429	4383	4463	4385	4276	4047	4061	3939	3998	4060	3976	3829
60	3656	3737	3717	3671	3740	3669	3591	3482	3514	3575	3419	3495	3504	3514	3538	3453	3525	3465	3429	3537
80	3553	3573	3592	3558	3519	3625	3610	3573	3622	3671	3629	3578	3605	3560	3593	3568	3565	3555	3552	3352
100	3573	3419	3417	3408	3456	3333	3402	3274	3340	3269	3158	3192	3265	3193	3131	3143	3122	3139	3050	2963
120	3048	2908	2906	2823	2855	2790	2609	2768	2825	2763	2711	2689	2712	2611	2595	2426	2566	2629	2519	2496
140	2490	2483	2429	2396	2383	2373	2298	2310	2306	2202	2281	2251	2354	2097	2046	2030	1996	1920	1787	1822
160	1731	1744	1730	1658	1577	1564	1484	1372	1323	1205	1228	1242	1093	1082	1051	956	915	988	946	952
180	910	896	882	939	924	921	892	931	850	843	881	867	874	878	903	787	888	809	836	893
200	857	804	837	872	834	830	864	933	879	916	928	946	959	1024	1070	1060	1117	1135	1246	1167
220	1285	1256	1270	1297	1362	1350	1394	1373	1457	1454	1442	1474	1504	1437	1484	1576	1529	1500	1579	1571
240	1585	1567	1659	1591	1634	1691	1631	1635	1581	1729	1609	1678	1681	1662	1611	1650	1722	1702	1758	1694
260	1629	1668	1630	1728	1628	1724	1739	1750	1586	1712	1667	1652	1672	1670	1725	1691	1569	1434	1316	1139
280	786	513	337	221	165	121	93	66	56	43	40	28	9	7	6	4	3	0	3	4
300	1	2	6	2	1	2	1	2	1	2	2	1	3	1	3	2	1	1	1	2
320	3	1	1	0	2	0	1	1	1	1	0	1	0	2	0	2	1	3	3	1
340	1	2	1	0	2	0	0	1	2	0	1	0	0	0	1	1	1	1	0	1
360	2	0	1	2	0	1	0	1	1	1	1	0	0	2	1	0	0	0	1	0
380	1	0	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
400	0	0	0	0	0	0	0	0	0	3	0	1	0	0	0	0	0	0	0	1
420	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
440	0	0	0	0	2	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
460	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
480	0	0	0	0	1	0	0	0	0	0	1	1	0	15	128	657	2348	5594	9644	8335
500	5297	2167	526	96	13	4	1	0	0	0	0	0								

University of Surrey

Department of Electronic and Electrical Engineering
Solid State Devices and Ion Beam Technology
Ion Beam Analysis and Implantation

k25103.rbs
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Mon Apr 17 12:45:31 1989

LCharge 10.0470 uC Chopper Counts 138657
LTime 1075.8 secs RTime 1091.0 secs

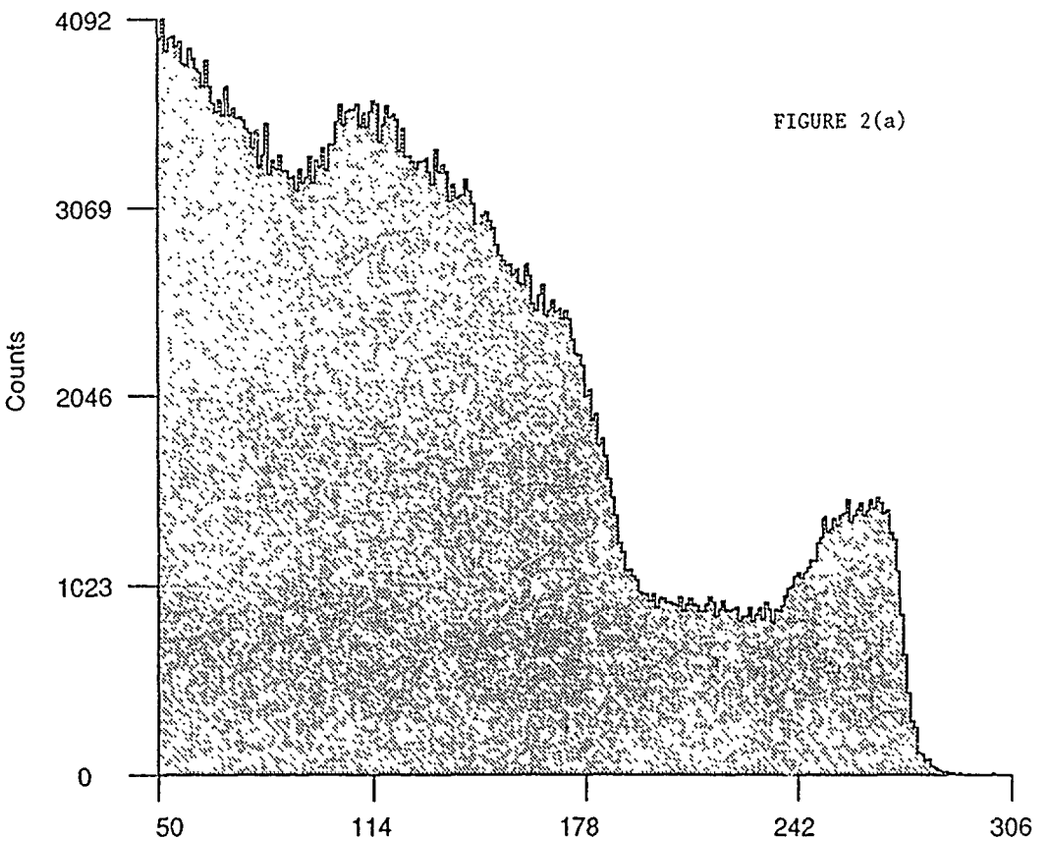


FIGURE 2(a)

Channel Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
40	0	0	0	337	1933	3071	3297	3727	3933	3943	3984	4093	3915	3990	4005	3946	3972	3855	3864	3938
60	3876	3825	3803	3727	3675	3736	3633	3591	3651	3572	3718	3567	3606	3548	3559	3559	3497	3475	3390	3483
80	3289	3356	3525	3250	3325	3279	3352	3247	3210	3236	3234	3165	3283	3207	3237	3348	3204	3326	3287	3395
100	3271	3413	3407	3529	3431	3517	3392	3402	3599	3424	3504	3578	3510	3592	3443	3631	3420	3516	3414	3555
120	3566	3540	3373	3500	3350	3342	3316	3282	3317	3315	3327	3265	3195	3388	3246	3298	3263	3099	3134	3114
140	3132	3135	3225	3156	3094	2982	2980	3025	3041	2934	2948	2869	2812	2702	2758	2761	2711	2732	2665	2654
160	2758	2698	2544	2511	2592	2468	2465	2514	2565	2502	2515	2465	2510	2465	2347	2272	2271	2210	2041	2075
180	1913	1946	1781	1820	1716	1603	1499	1404	1257	1209	1099	1109	1079	1057	993	979	978	946	985	908
200	954	954	938	937	928	912	958	886	922	953	916	915	888	885	920	942	938	863	895	947
220	884	884	898	910	829	858	862	910	832	871	896	836	931	896	823	897	889	919	969	1011
240	1020	1078	1095	1064	1096	1118	1158	1163	1256	1285	1388	1310	1330	1380	1345	1399	1410	1490	1370	1405
260	1432	1472	1399	1430	1485	1442	1499	1467	1410	1432	1297	1271	1102	866	649	485	292	262	129	119
280	79	69	50	45	34	25	21	12	10	6	8	5	4	6	7	6	5	5	3	4
300	2	2	3	3	1	7	3	3	5	7	3	2	5	3	5	5	3	3	4	3
320	4	2	1	0	0	3	1	2	1	0	3	0	2	1	4	0	1	1	0	1
340	0	1	1	2	0	3	0	3	2	1	0	2	0	1	0	0	0	0	1	1
360	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	2
380	0	1	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0
400	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1
420	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0
440	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
460	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
480	0	0	0	0	0	0	1	0	0	0	2	13	356	3708	15070	21773	10912	1913	157	7
500	5	2	0	3	0	4	3	2	2	2	3	3								

REPORT 2.

AFOSR-88-0356

UNIVERSITY OF SURREY

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Total Dielectric Isolation (TDI) of Fully Depleted Device Structures

P L F Hemment
July 1989

SECOND PROGRESS REPORT

ABSTRACT

The initial experiments described in the First Progress Report have provided a sound base for this project and further good progress has been made during this second reporting period in the areas of preparation of substrates, cross-sectional TEM analysis, computer modelling and materials science experiments. Delivery from the manufacturers of the heated sample holder is a few weeks behind schedule due to late delivery of components from a sub-contractor.

1. OBJECTIVE

The aim of this programme is to prepare, evaluate and optimise TDI structures as quickly as possible in order to develop the technology for the preparation of substrates for circuits which exhibit improved radiation tolerance. TDI structures incorporating N^+ implantation will additionally be examined.

2. TECHNICAL PROGRESS (April 1989 - June 1989)

2.1 Preparation of Substrates

A further two patterned 3" (100) silicon substrates have been successfully implanted. These have TDI FET test patterns etched in the poly-silicon masks of 0.25 μm (transparent to 200 keV O^+ ions) and 1.5 μm (opaque) thicknesses. These substrates have been returned to NRL, Washington, for capping, annealing and fabrication of test devices.

New materials science experiments have been started with the aim of evaluating TDI structures formed by the synthesis of a Si_3N_4 layer. This is supported by 200 keV N^+ implants into SiO_2 masked wafers. The patterned oxide layers are 0.31 μm and 0.47 μm thick and the implanted doses are 0.4×10^{18} N^+ cm^{-2}, 1.0×10^{18} N^+ cm^{-2} and 1.4×10^{18} N^+ cm^{-2}.

2.2 Microstructure of "as Implanted TDI Structures"

Cross-sectional samples prepared from an "as implanted" (no post implantation anneal) wafer (NRL Wafer Number 5) have been examined in a JEOL 200CX TEM. This wafer has a patterned poly-silicon mask of nominal thickness 2500 Å above a Si_3N_4 buffer layer of thickness 320 Å. These were deposited on a screen oxide of nominal thickness 210 Å.

Figure 1 shows a schematic of the actual structure together with a cross-sectional micrograph from which the layer thicknesses were determined. The edge of the mask is non-ideal having a slope of ≈45° in the lower part but is steeper near the top surface. The Si_3N_4 has been incompletely etched and extends about 0.45 μm into the window region.

An unannealed TDI structure formed by a dose of 1.8×10^{18} O/cm^2 is shown in Figure 2, which includes a schematic of a typical structure and TEM micrographs from representative areas. Surprisingly, within the window region the silicon surface is ≈500 Å below the plane of the original surface which is still preserved and can be seen under the field mask. Within the field region the structure consists of 1400 Å of polysilicon, about 600 Å of buffer layer, 1400 Å of defective but crystalline silicon, 2900 Å of amorphous oxide and 2000 Å of highly defective silicon above the silicon substrate. As a negligible amount of oxide is deposited in the polysilicon the change in thickness is due solely to sputtering which gives a sputtering coefficient for 200 keV O^+ ions at 550°C of 0.22 atoms/O atom. Within the window region the structure consists of 3500 Å of defective single crystal silicon, 2900 Å of amorphous oxide, about 2000 Å of damage silicon above the silicon substrate. As predicted the amorphous oxide layer has the same thickness (2900 Å) in both the field and window regions.

The edge of the window shows a smooth transition between the geometries of the field and window structures. It is noted that sputtering of the mask has reduced the slope of the mask edge. Finger like protrusions of defective silicon penetrate into the synthesised layer of SiO_2. A silicon rich region has been reported previously[1] in wafers with an oxide mask and this phenomena is associated with the lateral movement of the window edge due to sputtering. The effect is less pronounced in this polysilicon masked wafer and it is anticipated that oxygen segregation during high temperature annealing will achieve good dielectric isolation between the silicon device island and substrate.

Conclusions which may be drawn from these experiments include:

(a) desirability of a thicker polysilicon mask (3000 Å) to achieve a field oxide extending up to the silicon surface,

(b) sputter coefficient for 200 keV O^+ in polysilicon (550°C) is 0.22 atoms per ion (the measured rate for SiO_2 is 1.1 atom per ion with theoretical (TRIM) values of 0.18 and 0.38, for Si and SiO_2, respectively),

(c) the improved edge structure may be due to the lower sputtering rate of polysilicon compared to SiO_2,

(d) it is desirable to have vertical mask edges, and

(e) the Si_3N_4/SiO_2 buffer layer maintains its integrity during O^+ implantation.

Additional specimens implanted with a higher dose (2.4×10^{18} O cm^{-2}) have been thinned and are ready for examination in the TEM.

2.3 Materials Science Experiments

2.3.1 Stoichiometry

Previous analyses by SIMS[1] of oxides formed beneath an oxide mask have suggested that the layer is not stoichiometric SiO_2 but rather SiO_x where $x \approx 1.7$. Preliminary RBS analysis, recorded in the first report, seemed to support the SIMS data. During this reporting period very detailed RBS analyses have been carried out to achieve a more reliable measure of the value of x and to support the computer modelling (Section 2.4). It is important to note that this new data clearly shows the oxide is stoichiometric ($x = 2.00 \pm 0.05$) to within experimental errors. The reason for the discrepancy between SIMS and RBS analyses is not obvious but as ion yields are known to be influenced by the matrix it is reasonable to accept the new RBS data described below.

Figure 3 shows 1.5 MeV He^+ RBS spectra from a thick polysilicon layer (1.5 μm), a standard SIMOX sample implanted with 1.8×10^{18} O^+ cm^{-2} at 200 keV and a TDI test structure in which 1.8×10^{18} O^+ cm^{-2} were implanted through an SiO_2 mask of thickness 3200 Å. Figure 4 shows RBS simulation spectra for (i) bulk silicon, (ii) 3000 Å silicon on 3000 Å SiO_2 on silicon, and (iii) 2000 Å silicon on 3000 Å SiO_2 on silicon. The data is consistent and by taking ratios of yields it is concluded that the oxide in the TDI sample has a stoichiometric composition (±2.5%).

2.3.2 Implantation into Polysilicon

Figure 5 shows 1.5 MeV He^+ RBS spectra from a wafer with a thin polysilicon mask (0.25 μm) and a Si_3N_4/SiO_2 buffer layer. The regions are labelled in the figure. The buffer layer has been used as a shallow buried marker and enables the sputtering coefficient of 200 keV O^+ into polysilicon to be estimated (0.22 atoms per ion).

Figure 6 confirms the formation of a buried layer of SiO_2 in the thick polysilicon film (1.5 μm) after implantation of 1.8×10^{18} O^+ cm^2.

2.4 Computer Modelling

Further refinements have been made to the computer model and simulations have been run to determine the sensitivity of the structure to the diffusion of excess oxygen in the buried oxide.

Figure 7 shows the evolution of the oxygen depth profile in bulk silicon over the dose range 0.6×10^{18} O^+ cm^{-2} to 2.6×10^{18} O^+ cm^{-2}. The sputter rate is 0.2 and excess oxygen is allowed to move to the upper (near surface) Si/SiO_2 interface. As expected this interface advances towards the surface and rapidly becomes more abrupt.

Figure 8(a), (b) and (c) show the evolution of the oxide profiles in samples with an oxide mask of thickness 3200 Å. The sputtering coefficient is 1.1 atoms per ion. Figures 8(a), (b) and (c) show profiles when excess oxygen diffuses to the lower interface, distributes equally and diffuses to the upper interface, respectively.

The following conclusions may be drawn:

(a) in SIMOX structures the oxygen peak moves away from the surface with increasing dose,

(b) for TDI samples the oxygen peak moves towards the free (upper) surface, the effect is independent of the direction of oxygen diffusion being dominated by sputtering of the mask, and

(c) the critical dose just to achieve a stoichiometric oxide is 1.35×10^{18} O^+ cm^{-2} for SIMOX and 1.57×10^{18} O^+ cm^{-2} for TDI structures.

2.5 Heated Sample Holder

Delivery of the heated sample holder (funded under another contract) has been delayed due to late delivery of components from a sub-contractor. Acceptance tests will be carried out during early August 1989 and it is planned to implant wafers using preheating during the next reporting period.

3. FUTURE WORKPLAN

Priorities during the next period will be:

(a) cross-sectional TEM analysis of annealed TDI structures,

(b) implantation of additional wafers for the fabrication of CMOS test structures at NRL,

(c) refinements to the computer model, to include thermal segregation,

(d) materials science, further measurements to quantify the effects of swelling and sputtering.

REFERENCES

(1) P L F Hemment et al, Nucl Inst Meths B37/38, 766 - 769, 1989.

Activity	July	August	Sept
XTEM analysis of the first batch of wafers annealed at Naval Research Laboratories.		———	
O^+ ion implantation.		———	———
Sample preparation and XTEM analysis.	———	———	———
Computer modelling.	———	———	
Definition of new structures.			———
Commission heated sample holder.		———	
Materials science experiments (eg RBS)	———	———	———
Electrical evaluation (NRL)		———	

Discussions will be held with our sponsors/collaborators to define improved structures and to agree upon future experiments to assess the electrical characteristics and radiation tolerance of the structures.

P L F Hemment
July 1989

FIGURE CAPTIONS

1. XTEM micrograph showing the edge of the thin polysilicon mask.

2. XTEM micrograph shown as-implanted structure ($D = 1.8 \times 10^{18}$ O^+ cm^{-2}, $E = 200$ keV, $T_i = 550°C$) in mask, transition and window region.

3. RBS profiles after implantation ($D = 1.8 \times 10^{18}$ O^+ cm^{-2}, $E = 200$ keV, $T_i = 550°C$) into silicon and through a 320 nm thick SiO_2 mask (remainder of oxide mask removed). The profile of the thick polysilicon mask is taken as a reference.

4. Theoretically expected RBS profiles for the layered structures shown in the schematics.

5. RBS profiles of the thin polysilicon sample (see schematic) before and after implantation ($D = 1.8 \times 10^{18}$ O^+ cm^{-2}, $E = 200$ keV, $T_i = 550°C$).

6. RBS profiles of the thick polysilicon sample (1.5 μm) before and after implantation ($D = 1.8 \times 10^{18}$ O^+ cm^{-2}, $E = 200$ keV, $T_i = 550°C$) in comparison to an implantation into bulk silicon.

7. Calculated θ-profiles for the implantation of different doses into silicon ($E = 200$ keV) with diffusion directed to upper interface.

8. Calculated θ-profiles for the implantation of different doses through a 320 nm thick SiO_2 mask. The diffusion is directed to (a) lower interface, (b) both interfaces, and (c) upper interface.

FIGURE 1

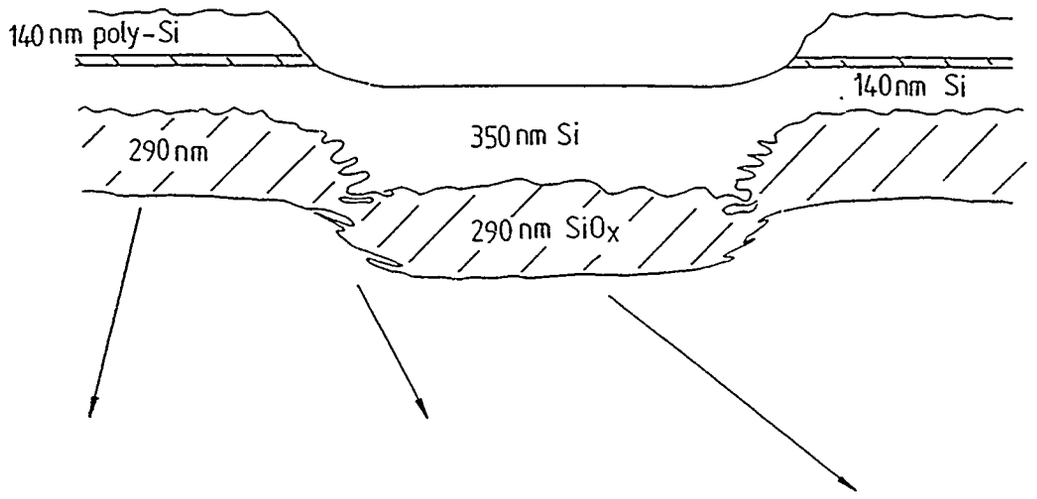


FIGURE 2

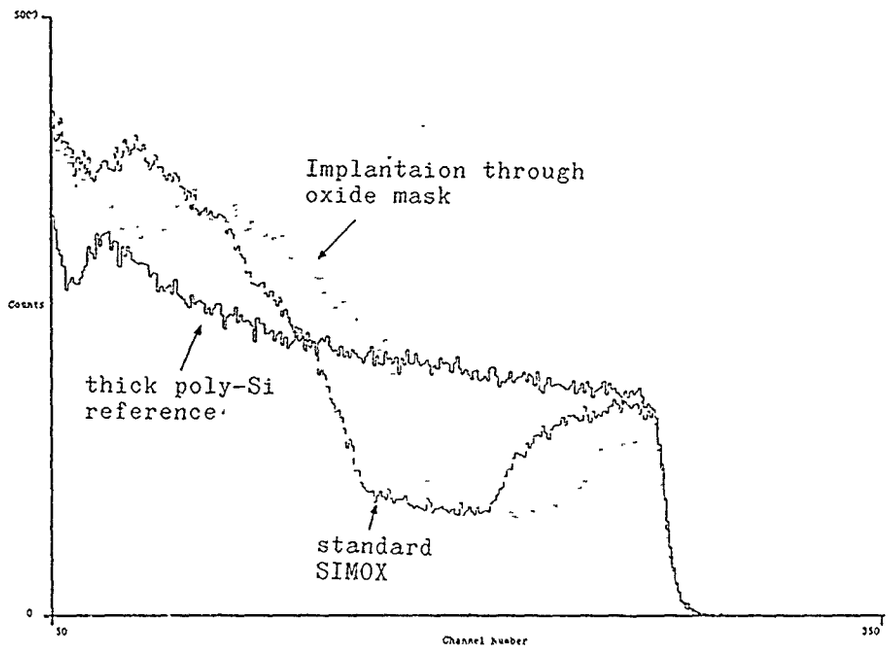
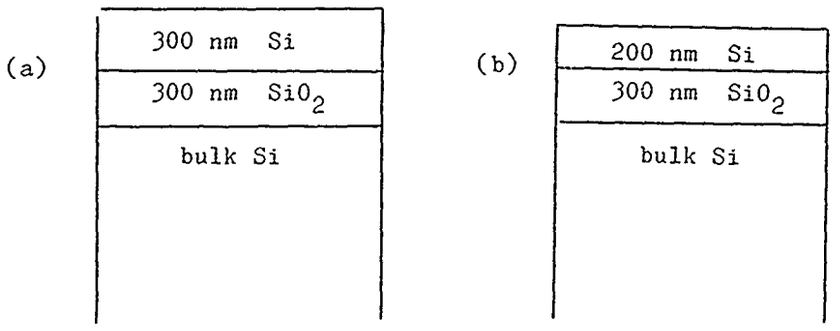

Implantaion through
oxide mask
thick poly-Si
reference
standard
SIMOX
Counts
0
50
350
Channel Number

FIGURE 3


(a)
300 nm Si
300 nm SiO_2
bulk Si
(b)
200 nm Si
300 nm SiO_2
bulk Si

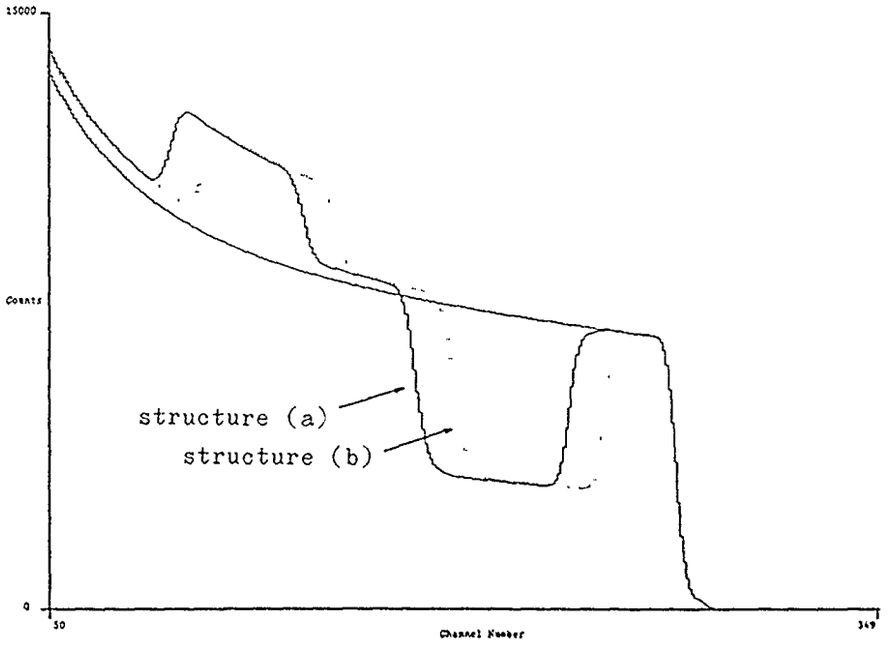
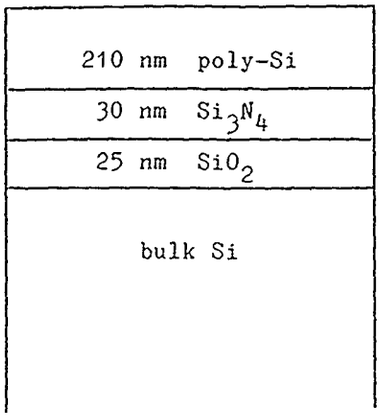

15000
Counts
0
50
Channel Number
349
structure (a)
structure (b)

FIGURE 4


210 nm poly-Si
30 nm Si_3N_4
25 nm SiO_2
bulk Si

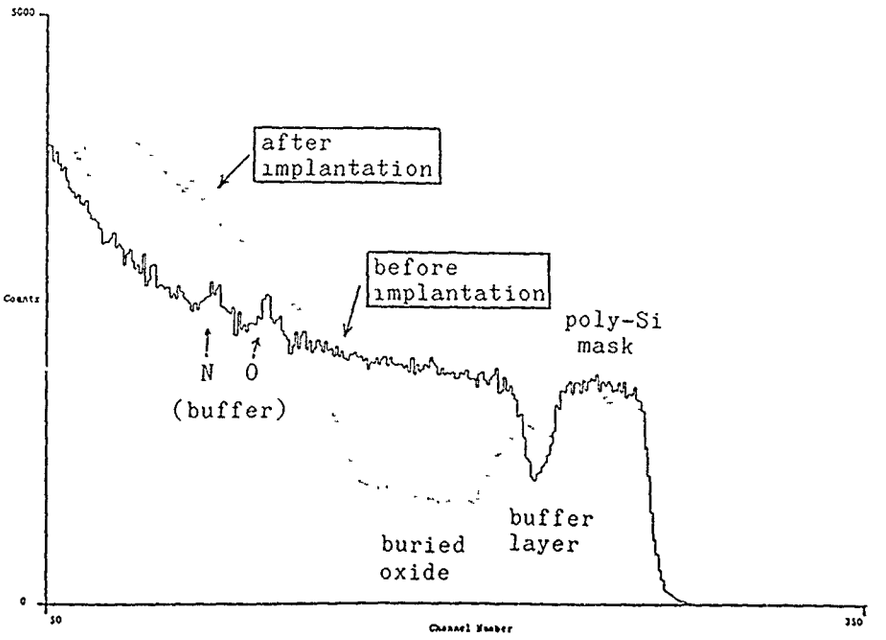

5000
0
50
310
after implantation
before implantation
poly-Si mask
N
O
(buffer)
buffer layer
buried oxide

FIGURE 5

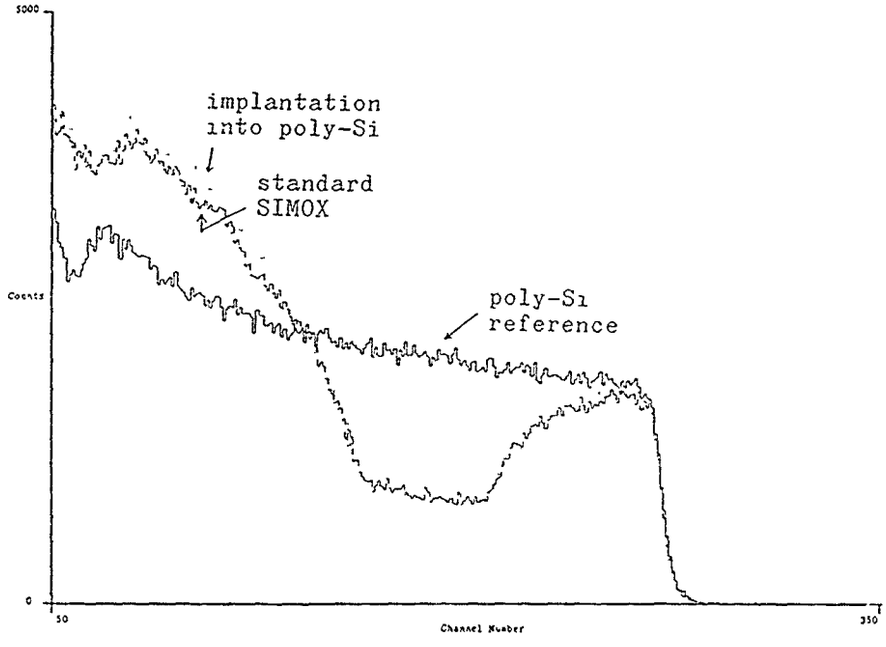

5000
implantation
into poly-Si
standard
SIMOX
poly-Si
reference
Counts
0
50
Channel Number
350

FIGURE 6

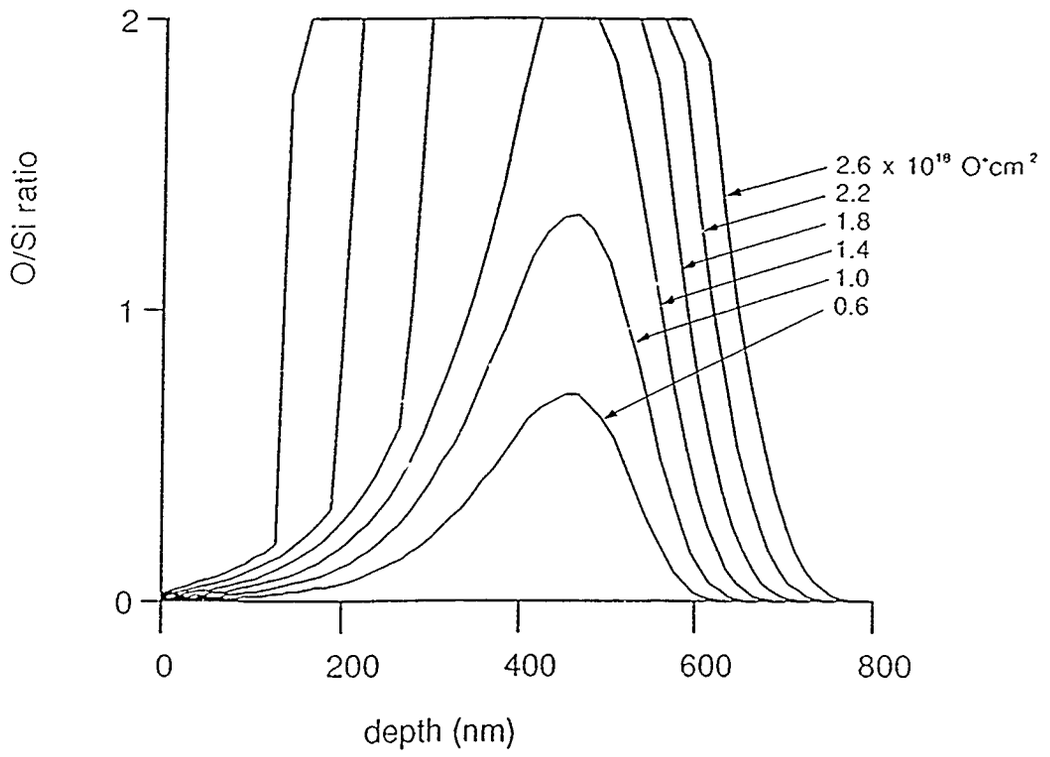

2
1
0
O/Si ratio
0
200
400
600
800
depth (nm)
2.6 x 10¹⁸ O·cm⁻²
2.2
1.8
1.4
1.0
0.6

FIGURE 7

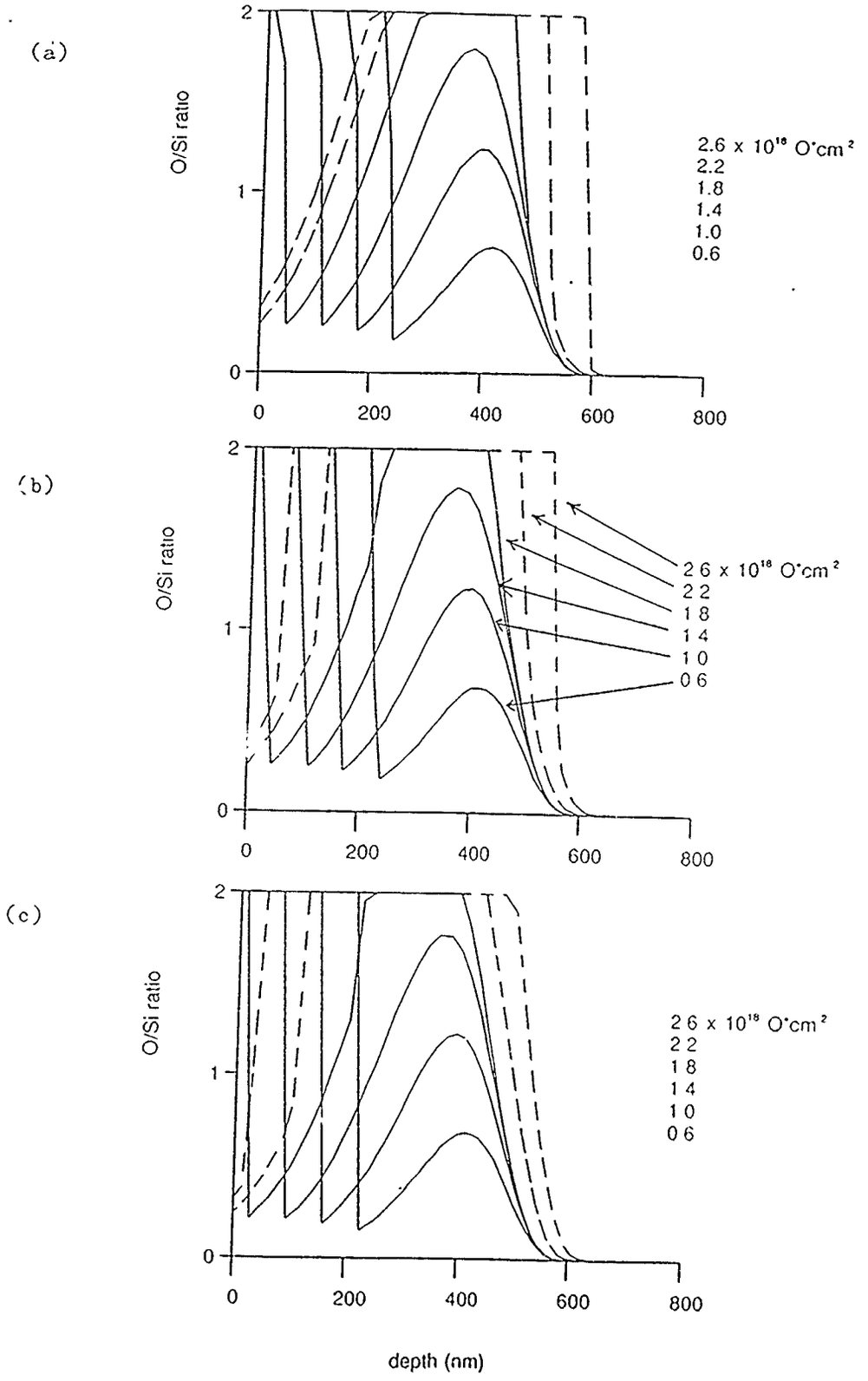

(a)
(b)
(c)
O/Si ratio
2
1
0
0
200
400
600
800
2.6 x 10¹⁸ O*cm²
2.2
1.8
1.4
1.0
0.6
2 6 x 10¹⁸ O*cm²
2 2
1 8
1 4
1 0
0 6
depth (nm)

FIGURE 8

REPORT 3.

AFOSR-88-0356

UNIVERSITY OF SURREY

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Total Dielectric Isolation (TDI) of Fully Depleted Device Structures

U Bussmann
June 1990

PROGRESS REPORT

1. REPORT FOR THE LAST PERIOD

Extensive testing of the heated sample holder, which was purchased under a separate contract has been carried out. 3" to 6" wafers can now be implanted in the temperature range 200 - 700°C (calibrated). The system is now in routine use for substrate preparation.

1.1 Heated Sample Holder

- Extensive testing: ok.
- Temperature calibration.
- Now in routine use for substrate preparation.

1.2 Substrate Preparation

A new set of twenty-one masked and patterned substrates has been fabricated by the NRL for materials science experiments: LOCOS oxide masks of 1920, 2565 and 3760 Å; SiO_2 masks of 2370, 3685 and 4389 Å; poly-Si masks of 2450 Å.

When the oxide mask is formed in a LOCOS process 55% of this masking layer is located above and 45% below the silicon surface level. As shown by simulations, a planar surface can then be achieved after implantation (see schematic in Figure 1). Also, the transition between the buried oxide layers in the mask and window regions will be smoother. Therefore, a structural improvement of the critical transition region is expected.

A different approach uses relatively low implantation energies to avoid steep steps between the oxides in the transition region. The lower flank of the implantation profile itself in the mask region as well as in the window region will be steeper due to the reduced straggle of the ion distribution. This might lead to the absence of silicon inclusions at the lower interface, which are always found under standard implantation conditions. The necessary wafer temperature can now be maintained by the background heating using the new sample holder. An additional advantage is the formation of a thinner silicon overlayer for fully depleted device areas.

A wafer with a LOCOS oxide pattern of 3760 Å has been implanted with 0.4, 1.8 and 2.2 x 10^{18} O$^+$ cm^{-2} at the standard energy of 200 keV/atom at the elevated temperature of 700°C, with background heating from an array of halogen lamps.

Wafers with a 2370 Å SiO_2 pattern and a 2450 Å SiO_2 pattern were implanted at a relatively low energy of 100 keV/atom with 0.3, 1.2 and 1.5 x 10^{18} O$^+$ cm^{-2}.

The wafers were sent to the NRL for capping and annealing.

1.3 Materials Science Results

Microstructure of annealed samples (poly-Si masks)

- "thin" poly-Si mask
  (energy 200 keV, annealing 1310°C for five hours)

Polycrystalline silicon masks have been successfully used to form continuous non-planar buried oxide layers. As an example Figure 2 shows the result of a 1.8 x 10^{18} O$^+$ cm^{-2} implantation through a 250 nm mask. As expected, after annealing dislocations are found in the silicon top layer and silicon inclusions in the oxide close to the lower interface. In addition a vertical chain of inclusions appears in the transition region. These inclusions might be avoided by decreasing the slope of the mask edge. A thin superficial silicon overlayer is left underneath the mask, which can be used as an etch stop when removing the remainder of the masking material.

- "thick" poly-Si mask
  (energy 200 keV, annealing 1310°C for five hours)

Figure 3 shows the transition region of a sample implanted with 1.8 x 10^{18} O$^+$ cm^{-2} after annealing. Silicon islands are formed, which are disconnected from the bulk material, although many silicon inclusions still exist in the transition region. In the mask region all the oxygen is stopped in the upper half of the thick poly-Si layer forming a continuous oxide. After removal of the thick poly-Si (including its "buried" oxide layer) such silicon islands could be used for building devices.

- LOCOS oxide mask
  (energy 200 keV, annealing 1300°C for four hours, oxide cap)

A wafer with a LOCOS oxide mask was obtained, under alternative funding, for a test implantation. Figure 4 shows first results after implantation of 1.8 x 10^{18} O$^+$ cm^{-2}, subsequent capping and annealing. Compared to the previous implantations using poly-Si masks less Si-inclusions are found on that "vertical chain". However, the edge of the mask region contains a high number of inclusions, although probably these would not be detrimental for the performance of devices built in the silicon islands. Apart from the surface dip in the transition region itself a nearly planar surface has been

achieved. A more detailed study of the resulting structures is on the way using masking patterns designed and prepared in collaboration with the NRL.

1.4 Computer Simulation

The programme IRIS (U Bussmann and P L F Hemment, Nucl Inst & Meths B47, 22, 1990) has now been further developed to model the effect of very high temperature (≥1300°C) annealing when the implantation profile is transformed into a rectangular profile. It has been shown, that oxygen transport occurs up the macroscopic concentration gradient as the system moves to reduce the total energy through the growth of large SiO_2 precipitates at the expense of small precipitates and eventually reaches thermal equilibrium with the segregation of all of the implanted oxygen at the buried oxide layer. This layer, thus, may be considered as a planar precipitate of infinite radius. The phenomenological approach used here does not attempt to simulate processes on an atomic scale, which lead to the thermal segregation. In our calculations all the implanted oxygen (ie the total fluence minus the small amount of oxygen, which is deposited close to the surface and subsequently lost by surface erosion) is bound within a stoichiometric SiO_2 layer. The justification for neglecting out-diffusion is that there is good agreement between predicted and measured layer thicknesses in structures which have been well characterised.

Profiles have been calculated over a wide range of fluences. Figures 5 and 6 summarize the resulting layer thicknesses for 200 keV and 150 keV ions. Experimental layer thicknesses, as determined from XTEM micrographs or SIMS profiles from the literature, have been included for comparison. Taking into consideration the scatter of the experimental data, there is good agreement between experiment and simulation.

An important method for producing low defect density silicon top layers involves sequential implantation and annealing. The programme IRIS has been used to make predictions of layer thicknesses after multiple step implantations in comparison with single step implantations. The implantation of 1.8×10^{18} O^+ cm^{-2} in three equal steps will be considered as an example. Figure 7a shows the implantation profile for a fluence of 0.6×10^{18} O^+ cm^{-2} together with the rectangular profile after thermal segregation during high temperature annealing. This layer structure is the target for the second implantation stage with the same fluence, resulting in the distributions shown in Figure 7b (before and after annealing), while the final oxygen distributions after the third implantation and annealing are shown if Figure 7c. For comparison, the implantation of 1.8×10^{18} O^+ cm^{-2} in a single step is included as Figure 7d. Using multiple implantation and annealing leads to steeper flanks in as-implanted profiles due to the previous thermal segregation. The simulation also shows that the buried oxide layer is shifted 35 nm towards the surface. This shift is due to the early existence of a stoichiometric layer, which leads to an increase of the amount of oxygen being

redistributed by diffusion.

2. FUTURE WORKPLAN

Priorities during the next period will be:

(a) Cross-sectional TEM analysis of TDI structures formed by implants through LOCOS oxide masks.

(b) Fabrication of additional wafers for the optimisation of the structural properties.

(c) Lower energy (100 keV) implants using the heated sample holder.

(d) Refinements of the computer model to extend the energy range to 50 - 300 keV (especially important for the simulations of the planned lower energy implantations).

3. FIGURE CAPTIONS

Figure 1: LOCOS oxide mask (schematic): Expected structure of the periphery of the window before and after implantation and annealing.

Figure 2: "Thin" poly-Si mask: Resulting structure of the transition region after implantation (1.8×10^{18} O$^+$ cm^{-2}) and annealing (1310°C for five hours).

Figure 3: "Thick" poly-Si mask: Resulting structure of the transition region after implantation (1.8×10^{18} O$^+$ cm^{-2}) and annealing (1310°C for five hours).

Figure 4: LOCOS oxide mask: Resulting structure of the transition region after implantation (1.8×10^{18} O$^+$ cm^{-2}) and annealing (1300°C for four hours).

Figure 5: Calculated depth of the maximum oxygen concentration (R_{max}) and interface positions for 200 keV implantations into silicon in comparison to experimental data from the literature (symbols).

Figure 6: Calculated depth of the maximum oxygen concentration (R_{max}) and interface positions for 150 keV implantations into silicon in comparison to experimental data from the literature (symbols).

Figure 7: Calculated oxygen concentration profiles after implantation (histograms) and high temperature annealing (rectangular profiles):

(a) 0.6×10^{18} O$^+$ cm^{-2}
(b) $2 \times (0.6 \times 10^{18}$ O$^+$ cm$^{-2})$
(c) $3 \times (0.6 \times 10^{18}$ O$^+$ cm$^{-2})$
(d) 1.8×10^{18} O$^+$ cm^{-2}, single implantation stage

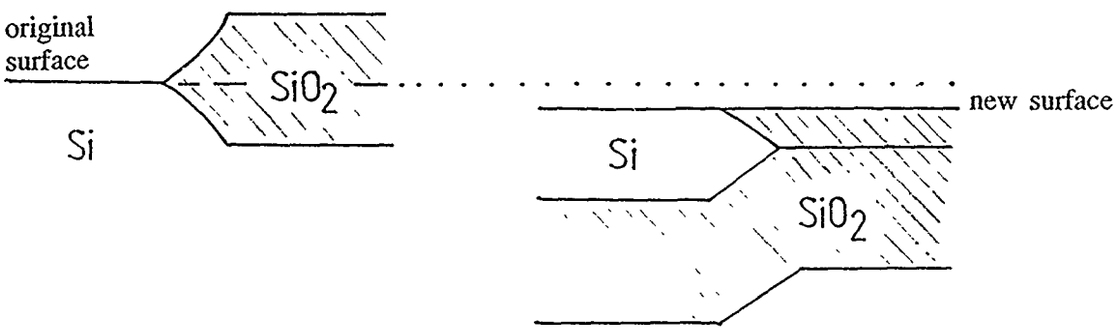

original
surface
Si
SiO_2
new surface
Si
SiO_2
before implantation
after implantation

Figure 1

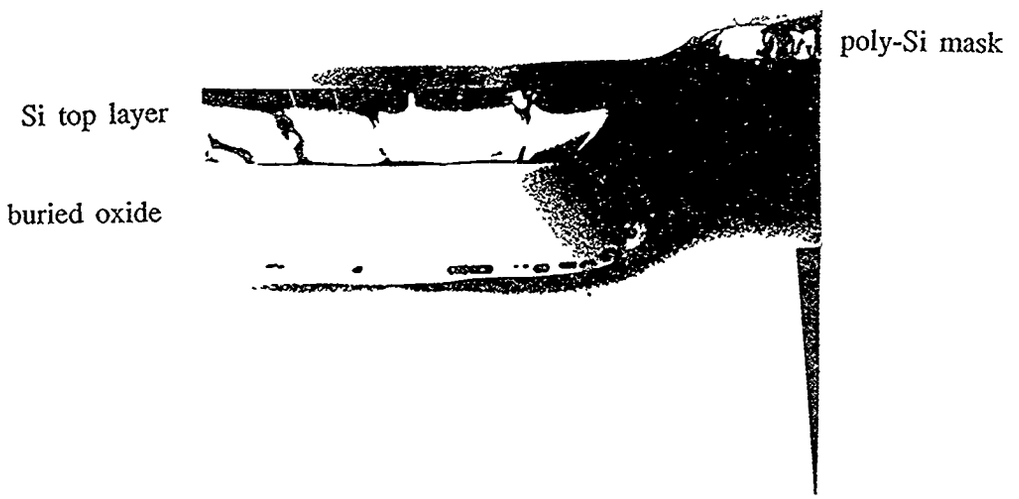


Figure 2

thick poly-Si mask
with implanted oxid

Si island

buried oxide

Figure 3


capping oxide
Si island
capping oxide
+ LOCOS oxide
+ implanted oxide

Figure 4

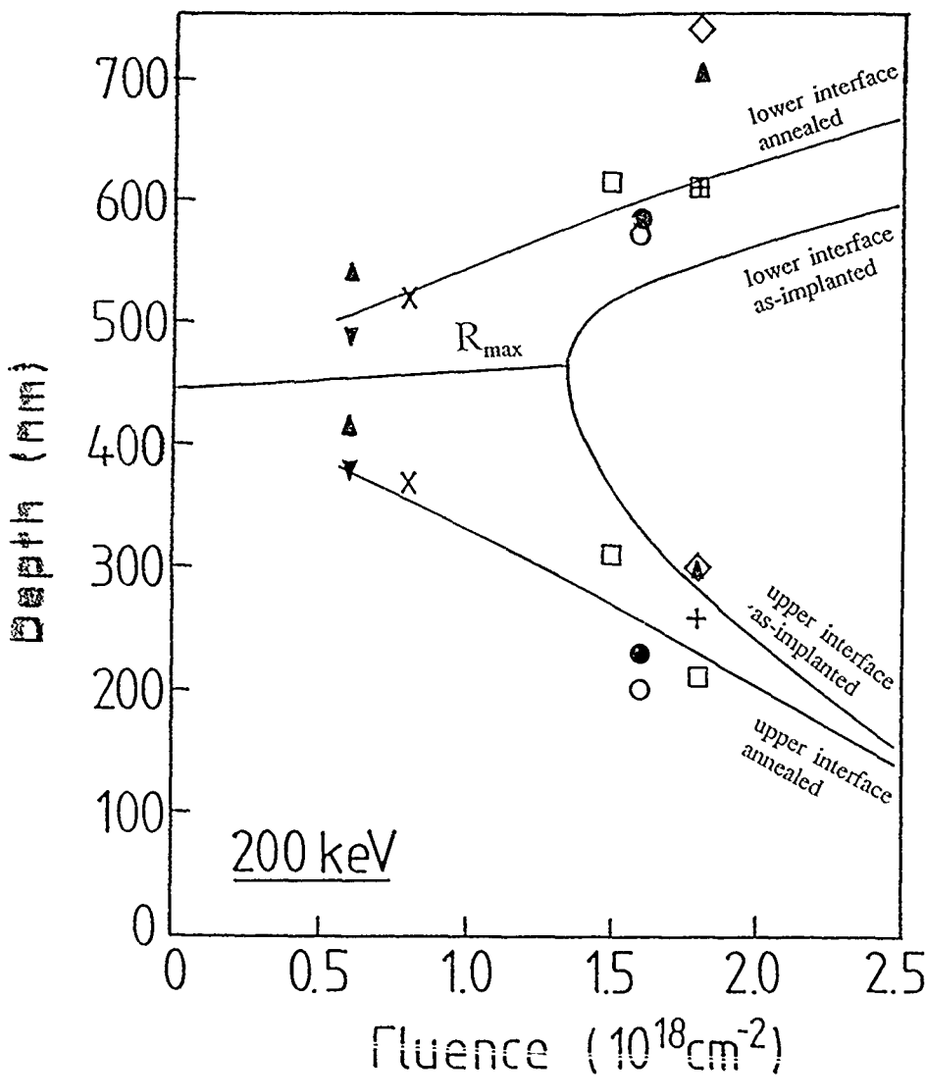

700
600
500
400
300
200
100
0
Depth (nm)
0
0.5
1.0
1.5
2.0
2.5
Fluence ($10^{18}cm^{-2}$)
lower interface annealed
lower interface as-implanted
R_{max}
upper interface as-implanted
upper interface annealed
200 keV

Figure 5

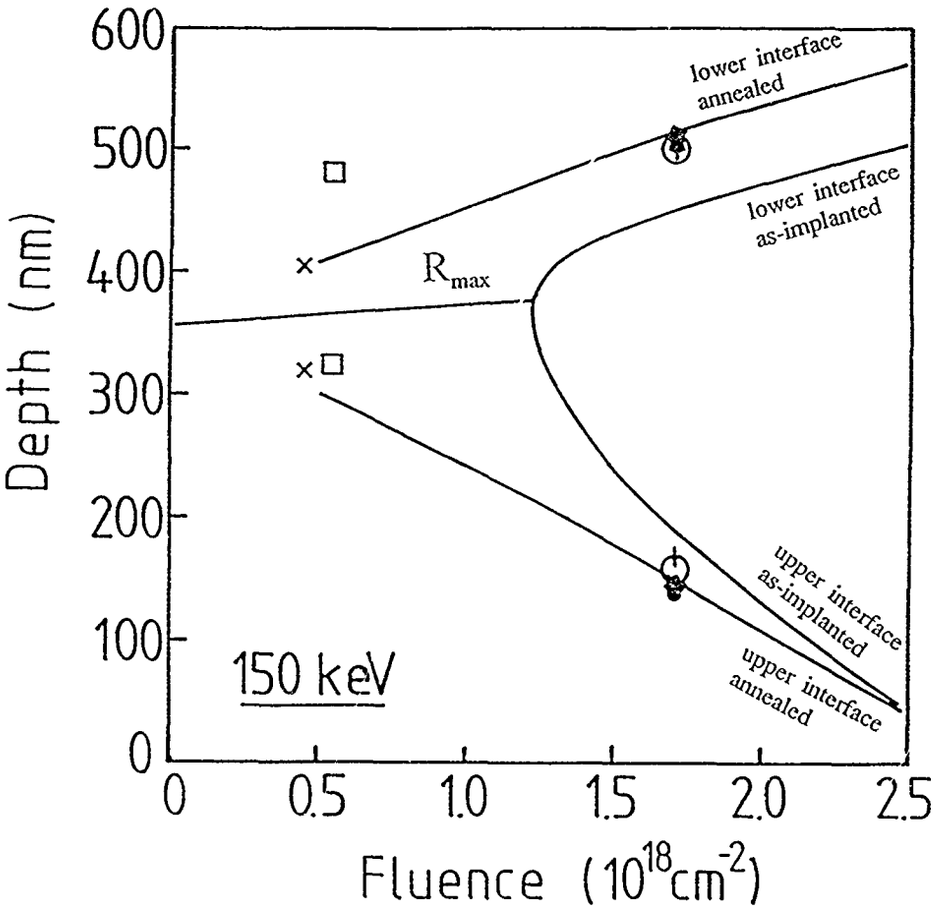

600
500
400
300
200
100
0
Depth (nm)
0
0.5
1.0
1.5
2.0
2.5
Fluence (10^{18}cm^{-2})
lower interface annealed
lower interface as-implanted
R_{max}
upper interface as-implanted
upper interface annealed
150 keV

Figure 6

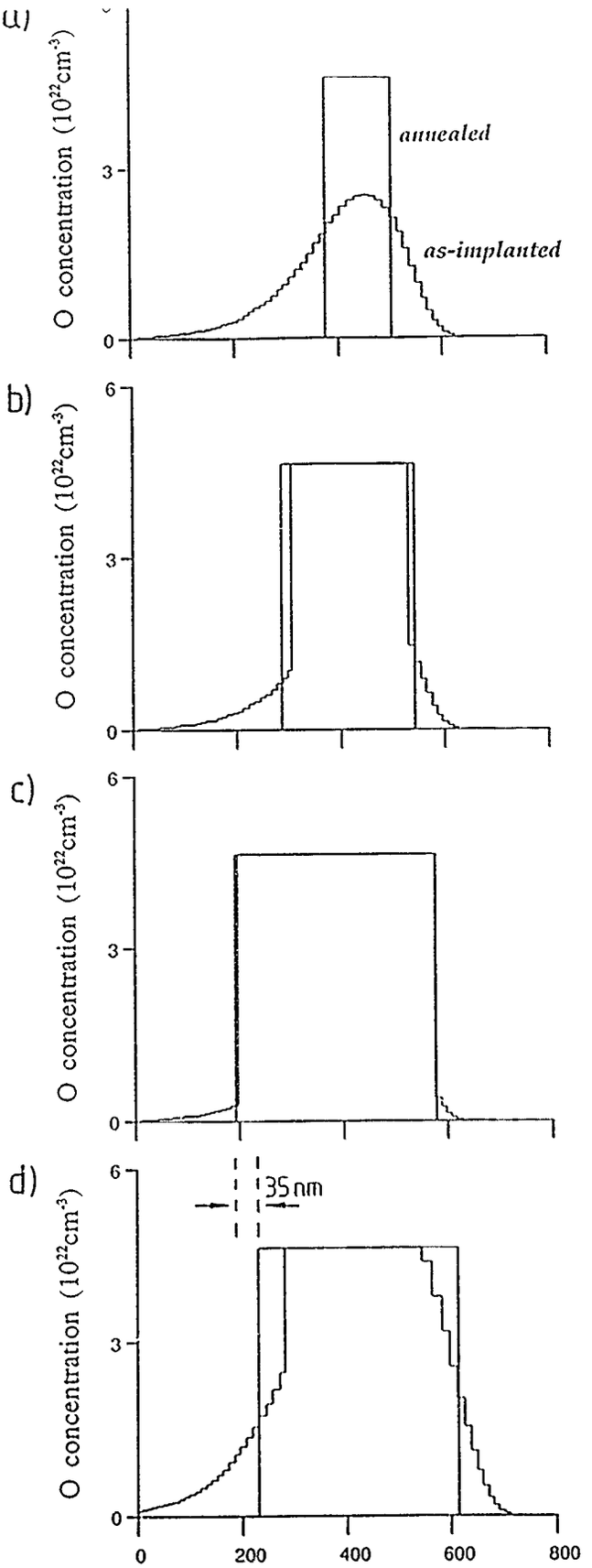

a)
O concentration (10^{22}cm^{-3})
annealed
as-implanted
b)
c)
d)
35 nm
0
3
6
0
200
400
600
800
depth (nm)

Figure 7